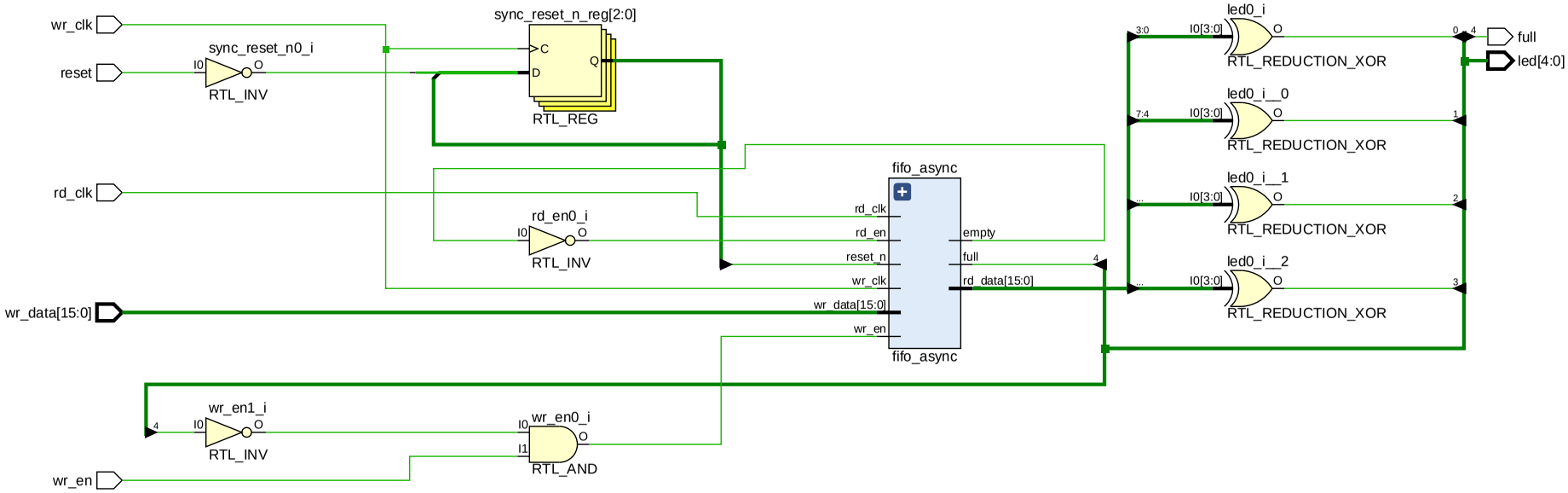
wr_clk
reset
sync_reset_n0_i
I0
O
RTL_INV
sync_reset_n_reg[2:0]
C
D
Q
RTL_REG
rd_clk
rd_en0_i
I0
O
RTL_INV
fifo_async
rd_clk
rd_en
reset_n
wr_clk
wr_data[15:0]
wr_en
empty
full
rd_data[15:0]
4
wr_data[15:0]
wr_en1_i
4
I0
O
RTL_INV
wr_en0_i
I0
I1
O
RTL_AND
wr_en
led0_i
3:0
I0[3:0]
O
RTL_REDUCTION_XOR
led0_i__0
7:4
I0[3:0]
O
RTL_REDUCTION_XOR
led0_i__1
...
I0[3:0]
O
RTL_REDUCTION_XOR
led0_i__2
...
I0[3:0]
O
RTL_REDUCTION_XOR
0
4
1
2
3
full
led[4:0]