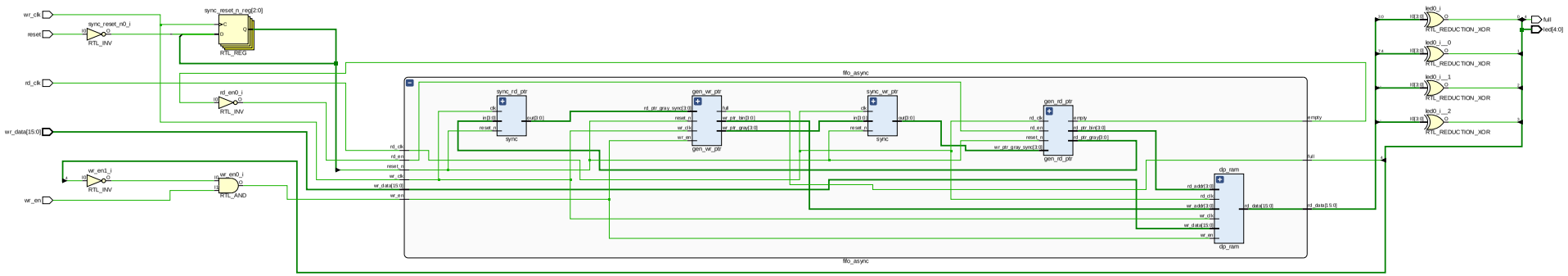
wr_clk
reset
rd_clk
wr_data[15:0]
wr_en
sync_reset_n0_i
RTL_INV
sync_reset_n_reg[2:0]
RTL_REG
rd_en0_i
RTL_INV
wr_en1_i
RTL_INV
wr_en0_i
RTL_AND
fifo_async
sync_rd_ptr
sync
gen_wr_ptr
sync_wr_ptr
sync
gen_rd_ptr
dp_ram
led0_i
RTL_REDUCTION_XOR
led0_i__0
RTL_REDUCTION_XOR
led0_i__1
RTL_REDUCTION_XOR
led0_i__2
RTL_REDUCTION_XOR
full
led[4:0]