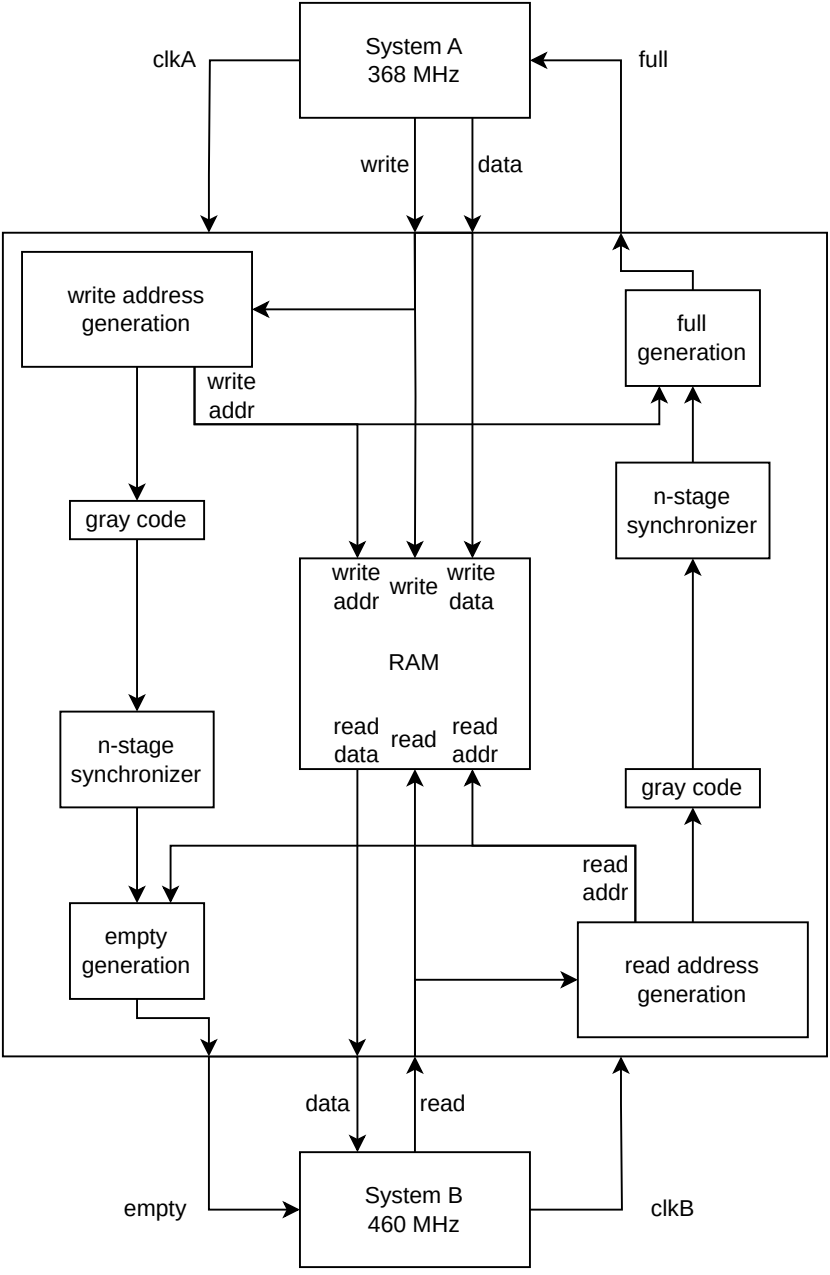
System A
368 MHz
clkA
full
write
data
write address generation
full generation
write addr
gray code
n-stage synchronizer
write addr
write
write data
RAM
read data
read
read addr
n-stage synchronizer
gray code
read addr
empty generation
read address generation
data
read
empty
System B
460 MHz
clkB