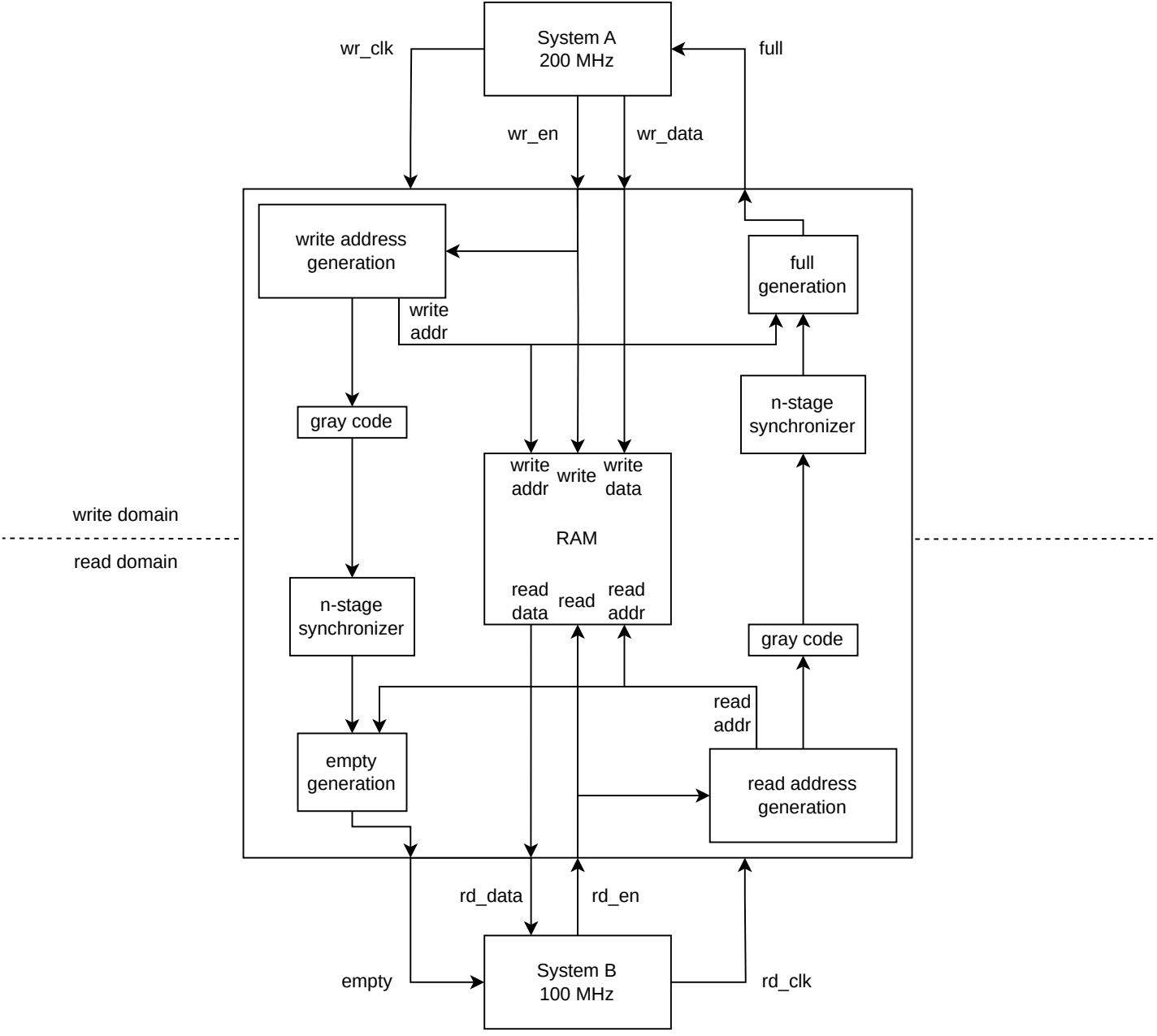
System A
200 MHz
wr_clk
full
wr_en
wr_data
write address generation
full generation
write addr
gray code
n-stage synchronizer
write addr
write
write data
RAM
read data
read
read addr
write domain
read domain
n-stage synchronizer
gray code
read addr
empty generation
read address generation
rd_data
rd_en
empty
System B
100 MHz
rd_clk