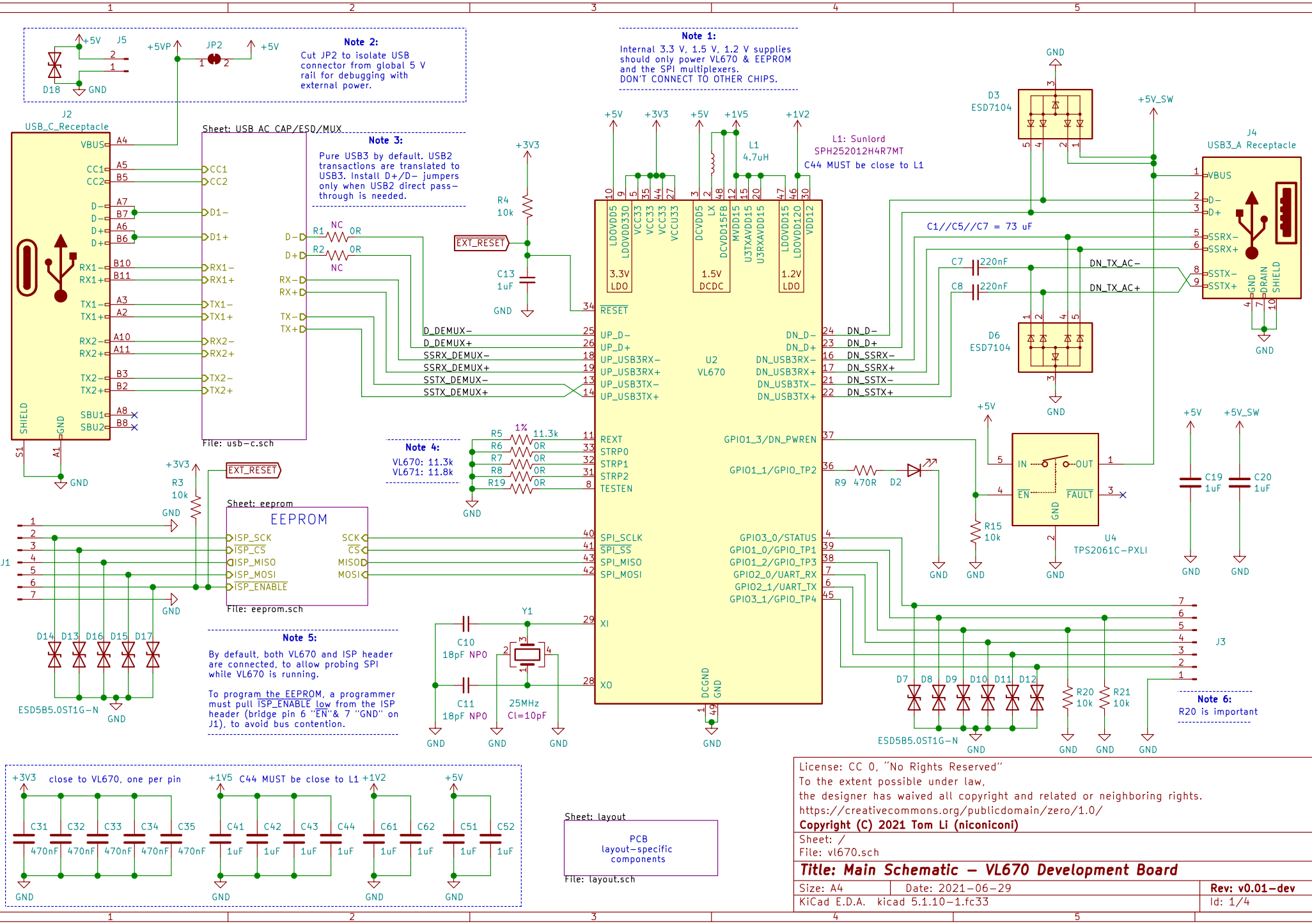
Note 2:
Cut JP2 to isolate USB connector from global 5 V rail for debugging with external power.
Note 1:
Internal 3.3 V, 1.5 V, 1.2 V supplies should only power VL670 & EEPROM and the SPI multiplexers.
DON'T CONNECT TO OTHER CHIPS.
Note 3:
Pure USB3 by default. USB2 transactions are translated to USB3. Install D+/D− jumpers only when USB2 direct pass−through is needed.
Note 4:
VL670: 11.3k
VL671: 11.8k
Note 5:
By default, both VL670 and ISP header are connected, to allow probing SPI while VL670 is running.
To program the EEPROM, a programmer must pull ISP_ENABLE low from the ISP header (bridge pin 6 "EN" & 7 "GND" on J1), to avoid bus contention.
Note 6:
R20 is important
L1: Sunlord SPH252012H4R7MT
C44 MUST be close to L1
C1//C5//C7 = 73 uF
U2 VL670
U4 TPS2061C−PXLI
J2 USB_C_Receptacle
J4 USB3_A Receptacle
Sheet: USB AC CAP/ESD/MUX
File: usb−c.sch
Sheet: eeprom
EEPROM
File: eeprom.sch
Sheet: layout
PCB layout−specific components
File: layout.sch
close to VL670, one per pin
C44 MUST be close to L1
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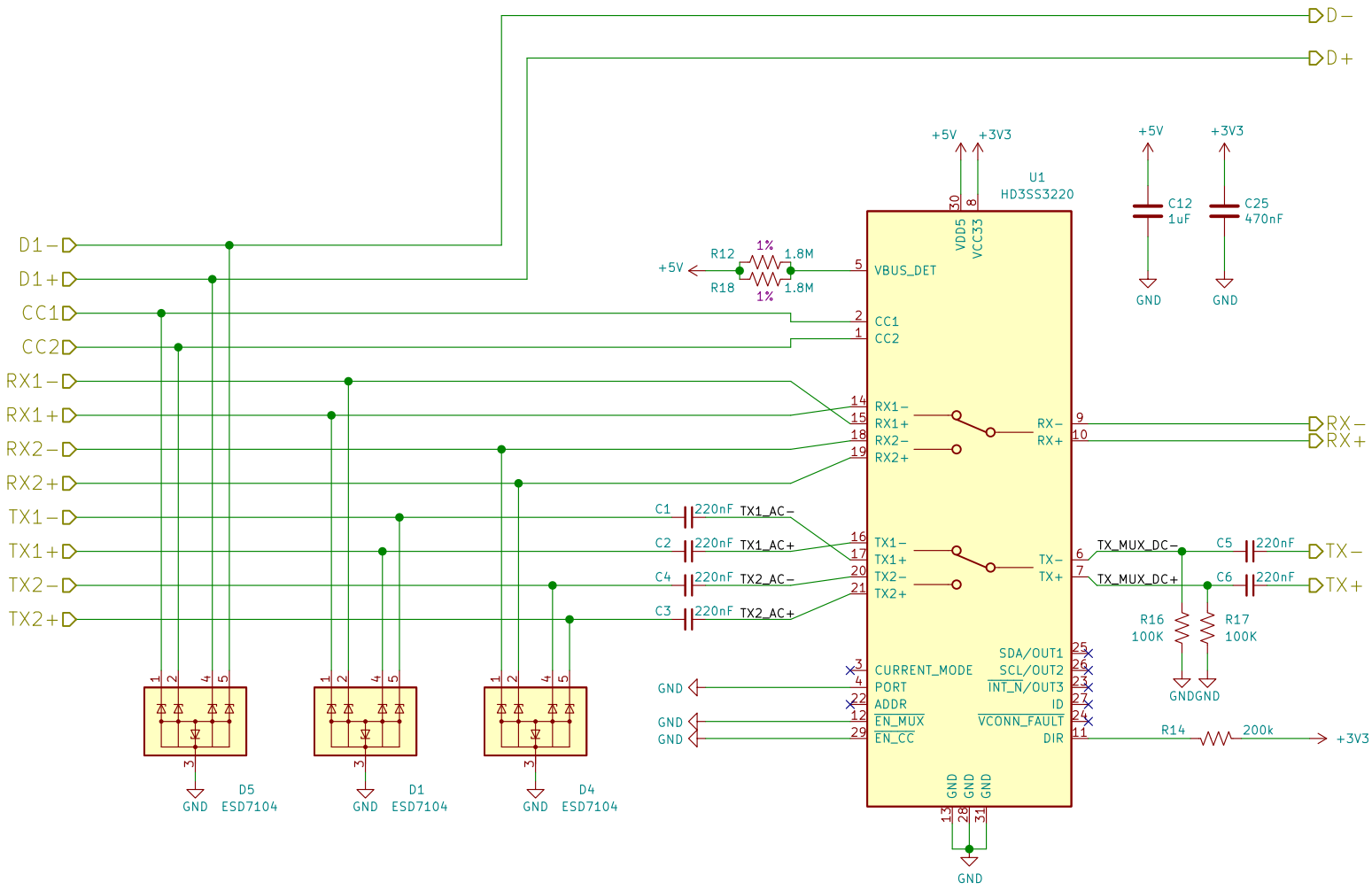
Sheet: /
File: vl670.sch
Title: Main Schematic − VL670 Development Board
Size: A4
Date: 2021−06−29
Rev: v0.01−dev
KiCad E.D.A. kicad 5.1.10−1.fc33
Id: 1/4



Note on TX−/TX+

The common−mode DC on RX and TX lines must be less than 2 V, but VL670 has up to 2.2 V DC at TX lines (RX lines are okay).

Thus, we need to block DC by C5 and C6, then use R16 and R17 to re−bias the operating point to 0 V.

C1/2/3/4 are always needed to block DC at the host. C5/6 and R16/17 are only needed when common−mode DC is greater than 2 V, like VL670.

Use 0402 or smaller for R16/17 to minimize stub.

originally for HD3SS3320, now deleted but keep it on board for stencil reuse.

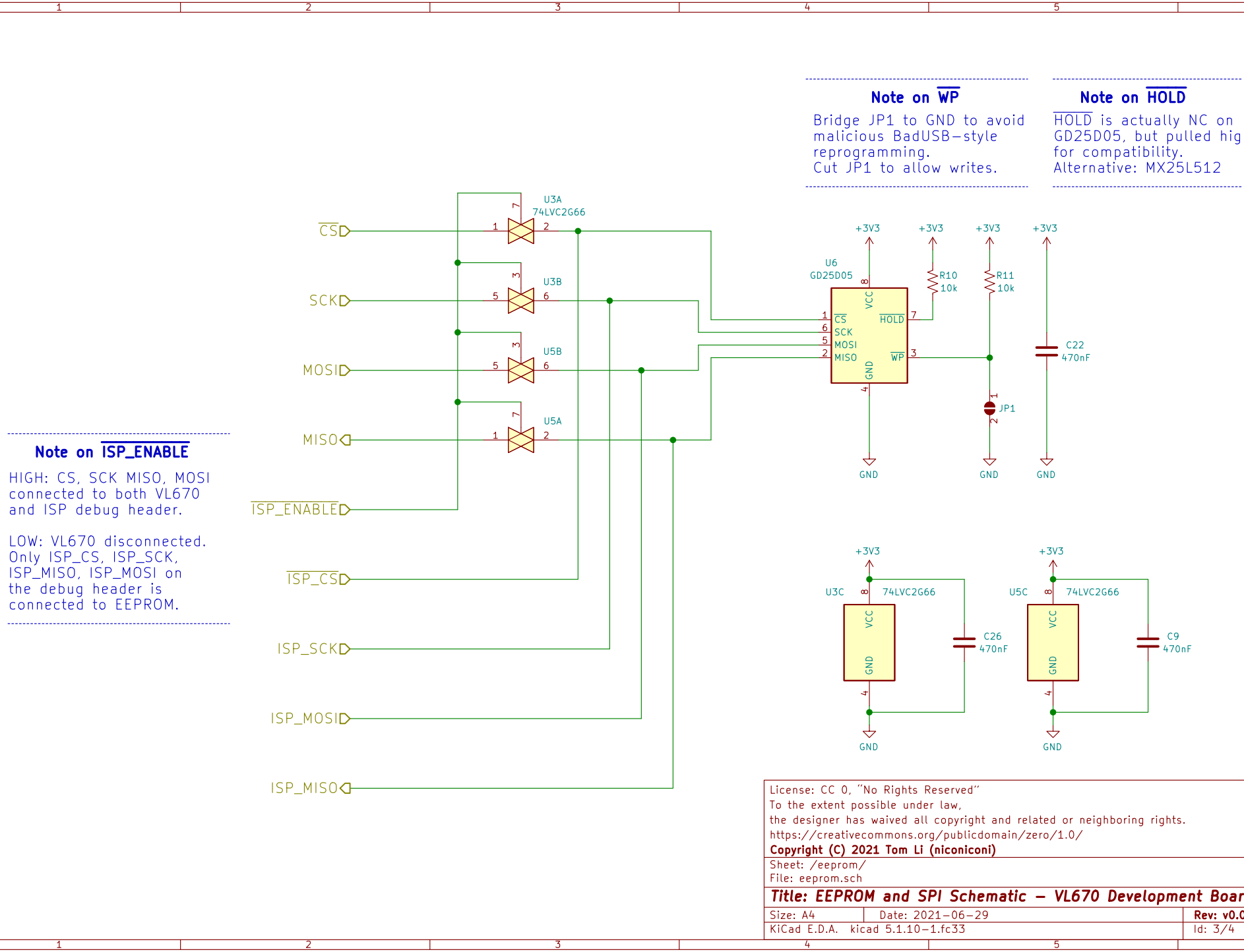
as a good practice, floating copper pads grounded.

you can use them as probe grounding points.

Sheet: /USB AC CAP/ESD/MUX/
File: usb−c.sch

Title: USB−C Schematic − VL670 Development Board

Size: A4	Date: 2021−06−29	**Rev: v0.01**
KiCad E.D.A. kicad 5.1.10−1.fc33		Id: 2/4


Note on WP
Bridge JP1 to GND to avoid malicious BadUSB−style reprogramming.
Cut JP1 to allow writes.
Note on HOLD
HOLD is actually NC on GD25D05, but pulled high for compatibility.
Alternative: MX25L512
Note on ISP_ENABLE
HIGH: CS, SCK MISO, MOSI connected to both VL670 and ISP debug header.
LOW: VL670 disconnected. Only ISP_CS, ISP_SCK, ISP_MISO, ISP_MOSI on the debug header is connected to EEPROM.
U3A
74LVC2G66
U3B
U5B
U5A
CS
SCK
MOSI
MISO
ISP_ENABLE
ISP_CS
ISP_SCK
ISP_MOSI
ISP_MISO
U6
GD25D05
+3V3
R10
10k
R11
10k
C22
470nF
JP1
GND
U3C
U5C
C26
C9
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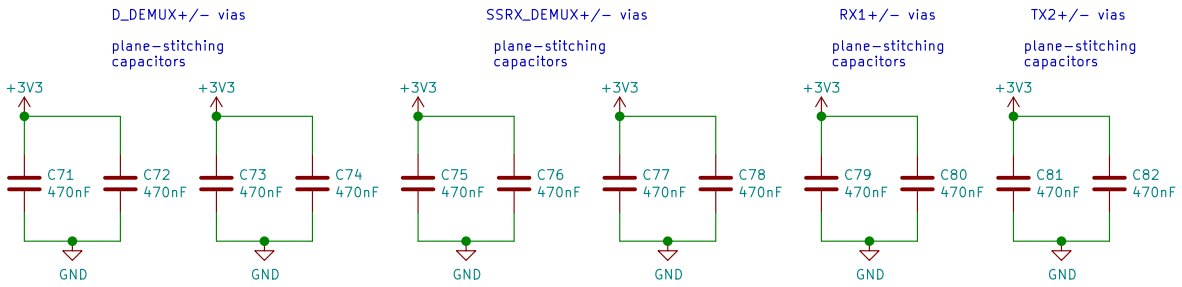
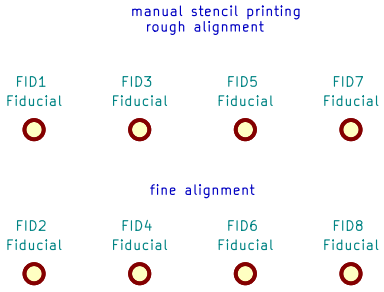
Sheet: /eeprom/
File: eeprom.sch
Title: EEPROM and SPI Schematic − VL670 Development Board
Size: A4
Date: 2021−06−29
Rev: v0.01
KiCad E.D.A. kicad 5.1.10−1.fc33
Id: 3/4





Sheet: /layout/
File: layout.sch

Title: PCB−specific Schematic − VL670 Development Board

Size: A4	Date: 2021−06−29	**Rev: v0.01**
KiCad E.D.A. kicad 5.1.10−1.fc33		Id: 4/4